STUDY OF 3-PHASE LINE COMMUTED THYRISTOR CONVERTER CIRCUIT

INTRODUCTION:

Single phase ac-to-dc converters are generally limited to a few kilowatts, and for higher levels of d.c. power output three-phase line commutated converters are used owing to restrictions on unbalanced loading, line harmonics, current surge and voltage dips. Increase in ripple frequency also reduces the filter size. converter which can be operated both in rectifying and inverter modes are called fully controlled converters. When power flow can only occur from ac-to-dc, the converter is known as semi converter, or half controlled converter. fully controlled three-phase converters find applications in high voltage dc power (HVDC) transmission, d.c. and a.c. motor drives with regenerative breaking capabilities.

AIM:

1. To observe various waveforms with R and R-L loads for both fully controlled and half controlled converters.
2. To plot graphs of mean load voltage against firing delay angles for R and R-L loads.
3. To study variation of power factor against delay angle.

CIRCUIT DESCRIPTIONS AND PRINCIPLES:

Fig. 5.5.1a shows the power circuit configuration of a three-phase fully controlled converter in which all the rectifying elements are thyristors. Fig5.5.1b shows the waveforms of supply voltages, converter output voltage under continuous load current condition, firing instants for controlling the output voltage and sequence of firing. Thyristors are gated on at an interval of 60° in the sequence in which they are numbered. Triggering angle \( \alpha \), also called firing delay angle, is defined with respect to the cross over points of the phase voltages at which an equivalent diode would start to conduct. In the positive group of thyristors, viz. \( T_{h1}, T_{h2} \) and \( T_{h3} \), turning on of one thyristor turns off a conducting thyristors in the group. So is the case with negative group of thyristors, viz. \( T_{h2}, T_{h4} \) and \( T_{h6} \). As a result with highly inductive load, carrying continuous current, each thyristor would conduct for a period of 120° in a cycle with commutation occurring every 60°.

Since at any instant two thyristors should be in the conducting state no current would flow if at start a single thyristor is given a pulse. This means that each thyristor should always be supplied with gate pulses 60° apart so that at start two thyristors can be triggered simultaneously.

Reference to Fig.5.5.1b shows that the ideal d.c. average output voltage (average height of the full line wave) of the converter under continuous load current is

\[
E_o = \frac{3\sqrt{2}}{\pi} E_{L-L} \cos \alpha
\]

Where \( E_{L-L} \) is the line to line rms voltage, and \( \alpha \) is the delay angle.
If thyristor drops and supply side inductances are taken into account, average load voltage is quite closely given by

\[ E_{oav} = E_o - 2V_{dc} - \frac{3\omega L_o}{\pi} I_L \]

where

- \( L_o \) = supply side inductance per phase
- \( \omega_o = 2\pi \) times the supply frequency
- \( I_L \) = average load current

For delay angle greater than 60°, the instantaneous output voltage will have a negative part in its periodicity for continuous load current (Fig 5.5.2a) with a resistive load current always in phase with voltage. As current through a thyristor cannot be negative, the output voltage cannot take any negative value. The range of control for delay angle \( \alpha \), with resistive load, is from 0° to 120°. For \( \alpha < 60° \), the ideal output voltage, with resistive load, is the same as in Fig.5.5.1b for continuous load current whereas for \( \alpha > 60° \), the output voltage waveform will be as shown in Fig.5.5.2b. The ideal average of the converter output voltage, with resistive load, is given by

\[ E_o = \frac{3\sqrt{2}}{\pi} E_{L-L} \left[ 1 + \cos \left( \frac{\alpha}{3} + \frac{\pi}{3} \right) \right] \text{ for } \frac{\pi}{3} < \alpha < \frac{2\pi}{3} \]

\[ = \frac{3\sqrt{2}}{\pi} E_{L-L} \cos \alpha \text{ for } 0 < \alpha < \frac{\pi}{3} \]

A fully controlled converter can be made a semi-converter by placing a freewheel diode across the load as shown in Fig.5.5.3. This circuit has the same output voltage characteristic as that of the full converter with resistive load since the output voltage can never go negative because of the freewheel diode. Another configuration of a three phase semi converter is a half controlled Converter bridge, shown in Fig.5.5.4a, where half the devices are thyristors, the Remainder being diodes. Thyristors get turned off either on the firing of another thyristor or by the action of the freewheeling diode. The circuit function will be the same with or without freewheeling diode. However, in order to avoid half waving effect in the case of trigger failure of the thyristors a freewheeling diode is a necessity. Fig.5.5.4b and 5.5.4c show the output voltage waveforms. For delay angle \( \alpha < \pi/3 \) output voltage wave is discontinuous. The average output voltage is given by

\[ E_o = \frac{3\sqrt{2}E_{L-L}}{\pi} \left( 1 + \cos \alpha \right) \text{ for } 0 < \alpha < \pi \]

A half-controlled converter, when compared to a fully controlled converter has no starting problems, but has higher harmonic content in the load voltage and the supply current waveforms.
TRIGGERING CIRCUIT:

The triggering circuit shown in Fig.5.5.5. for a fully controlled converter employs cosine wave control techniques so that the output voltage of the converter is proportional to the control voltage when the load current is continuous. The waveform at the output points of certain stages of the triggering circuit are shown in Fig.5.5.6. A set of three single phase transformer, connected in delta/ zig-zag (Fig.5.5.7) is used to obtain isolated low level synchronized balanced sinusoidal outputs $V_{g_1}$, $V_{g_3}$ and $V_{g_5}$ which lead the supply voltages $e_a$, $e_b$ and $e_c$ respectively by 60°. Phasor diagram in fig 5.5.7b explains the derivations of this 60° lead. Required subtractions are carried out on the secondary side of the transformer. Positive peaks of these voltages occur at the respective reference instants from which the delay angles for the positive group of the thyristors viz. $T_{h1}$, $T_{h2}$ and $T_{h5}$ are measured. This is illustrated in Fig. 5.5.6 for the voltage waveform $e_a$ and $V_{g1}$. Three inverters inverts $V_{g1}$, $V_{g3}$ and $V_{g5}$ to generate sine waves $V_{g2}$, $V_{g4}$ and $V_{g6}$ whose positive peaks occur at the respective reference instants from which delay angles for the negative group of thyristors viz. $T_{h2}$, $T_{h4}$ and $T_{h6}$ are measured.

Six separate but identical circuits are used for obtaining synchronized triggering pulses for the six thyristors and also for controlling their delay angles. Circuit description for generating the triggering pulses from the secondary phase voltage is only explained by reference to Fig.5.5.7. The circuit works as follows:

Signal voltage $V_{g1}$ is compared with a control voltage $v_c$ which can be controlled between $+V_m$ and $-V_m$ (peaks of $V_{g1}$). The differentiator network converts rectangular output of the comparator to trigger pulses for the input to the timer 555 which is wired for monostable operation. The monostable output is then fed through diodes to the supply and the reset pins (8 and 4) of two 555 timers. One timer belongs to the circuit under consideration and the other to the circuit appearing next in the sequence of firing. This is to ensure that two consecutive thyristors in the triggering sequence could receive gate firing signals simultaneously. These timers operate in astable mode, producing train of pulses over the period equal to the width of the monostable output. The modulated pulse signals from these astable multivibrators are fed to the pulse transformer and transistor based driver circuits, the outputs of which are the required triggering pulses for the thyristors.

PROCEDURE:

Triggering circuit:

- Construct the triggering control circuit as shown in Fig.5.5.5.
- Switch on the supply to the triggering circuit.
- Observe the waveforms at the output point of each stage up to the input of the driver circuit in relation to the sinusoidal input to the comparator. Use dual trace oscilloscope.
- Check polarity, pulse heights and phase displacement between output pulses at $g_1$ and $g_2$, $g_2$ and $g_3$ ............ $g_6$ and $g_1$. If the working of the circuit is as expected, 60° phase displacement between triggering pulses for two consecutive thyristors in the sequence of firing and two two pulses from each driver circuit will be obtained.
• Change the control voltage $V_c$ and see whether the pulses are shifting on block.

Converter circuit:

• Make the fully controlled converter bridge circuit as shown in Fig.5.5.8. Connect a suitable resistive load keeping in view the rating of the Thyristors.

• Before releasing the gate pulses to the thyristors to ensure that the Thyristors would be getting their respective triggering pulses on closing the gate switches $S_{W1}, S_{W2}, \ldots, S_{W6}$. Also ensure that the phase terminals of the incoming power supply are connected to the appropriate bridge arms.

• For an appropriately selected resistive load observe the wave forms of the output voltage, input current, line voltage at the bridge input terminals, and the thyristor voltage for two delay angles. One delay angle less than $\pi/6$ and the other greater than $\pi/6$.

• With the same resistive load vary the delay angle in suitable steps over its full range, and for each delay angle note the input power, supply current, average load voltage, rms and average load current.

• Add a suitable inductor, having time constant greater than 3ms in series with the resistive load. Repeat steps 3 and 4.

• Connect the converter as a half controlled three phase bridge (Fig.5.5.4a) and for a few specific delay angles and the same R and R-L load measure the input power, phase current, output voltage and load current (rms and average) and also note the same waveforms as indicated in step 3.

### Table 5.5.1
Experimental observation with semi converter/fully controlled converter

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Delay angle $\alpha$ Deg.</th>
<th>Input Power $W_1 + W_2$ watts</th>
<th>Input Current Amp.</th>
<th>Load voltage volts</th>
<th>Load current</th>
<th>Computed Output Voltage volts</th>
<th>Power factor</th>
</tr>
</thead>
</table>

Supply voltage = $V$
Load resistance = $\text{Ohms}$
Calculations and plots:

1. Trace or record, the various waveforms
2. Complete computations indicated in tables
3. For fully controlled converter plot on the same graph sheet, computed output voltage (eqn.5.5.1) and measured voltage against delay angles For both R and R-L loads.
4. Do same as above for half – controlled converter.
5. On the same graph paper plot power – factor against delay angle for fully Controlled and half – controlled converter.

Questions :

1. Why do notches and spikes occur in the waveform of line to line voltage at the input of the converter?
2. In which converter , fully controlled or half controlled, for the same output voltage ripple voltage is less?
3. For the same output voltage and power which converter, fully controlled or half controlled, requires lesss reactive power ?
4. What is the frequency of the lowest order harmonic in three-phase semi converters and that in three phase fully controlled converters?
5. Which converter has higher harmonic content in its load voltage and Supply current waveforms?

Circuit diagram
Common anode, common cathode and voltages with respect to supply neutral.
Fig. 5.5.2 Output voltage waveform of a full-wave three-phase controlled bridge converter. (a) Under continuous conduction mode for delay angle $\alpha > 60^\circ$, (b) with pure resistive load or with freewheel diode (vide Fig. 5.5.3).
Fig. 5.5.3 A full-wave three-phase controlled converter
With freewheel diode $D_F$

Fig. 5.5.4 Half-controlled three-phase bridge converter. (a) Circuit connection.
(b) Output voltage waveform: delay angle $\alpha < \pi / 3$.
(c) Output voltage waveform for delay angle $\alpha > \pi / 3$. 

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Fig. 3.3.6 Timing diagram - waveforms of certain points of the triggering circuit.
Fig. 5.3.7 Delta / Zig – zag transformer (a) Connection, (b) phasor diagram.